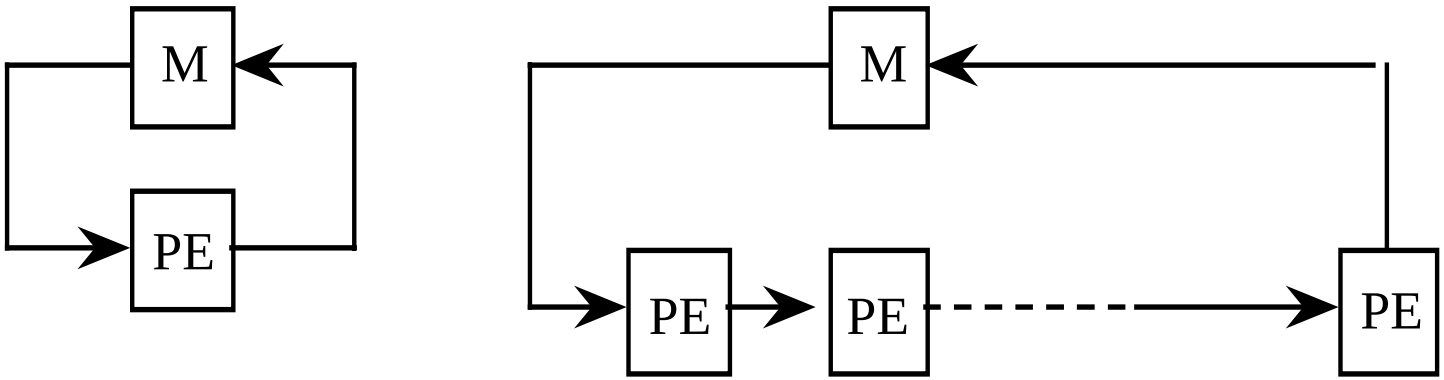
Slides from Shaaban

# Systolic Architectures

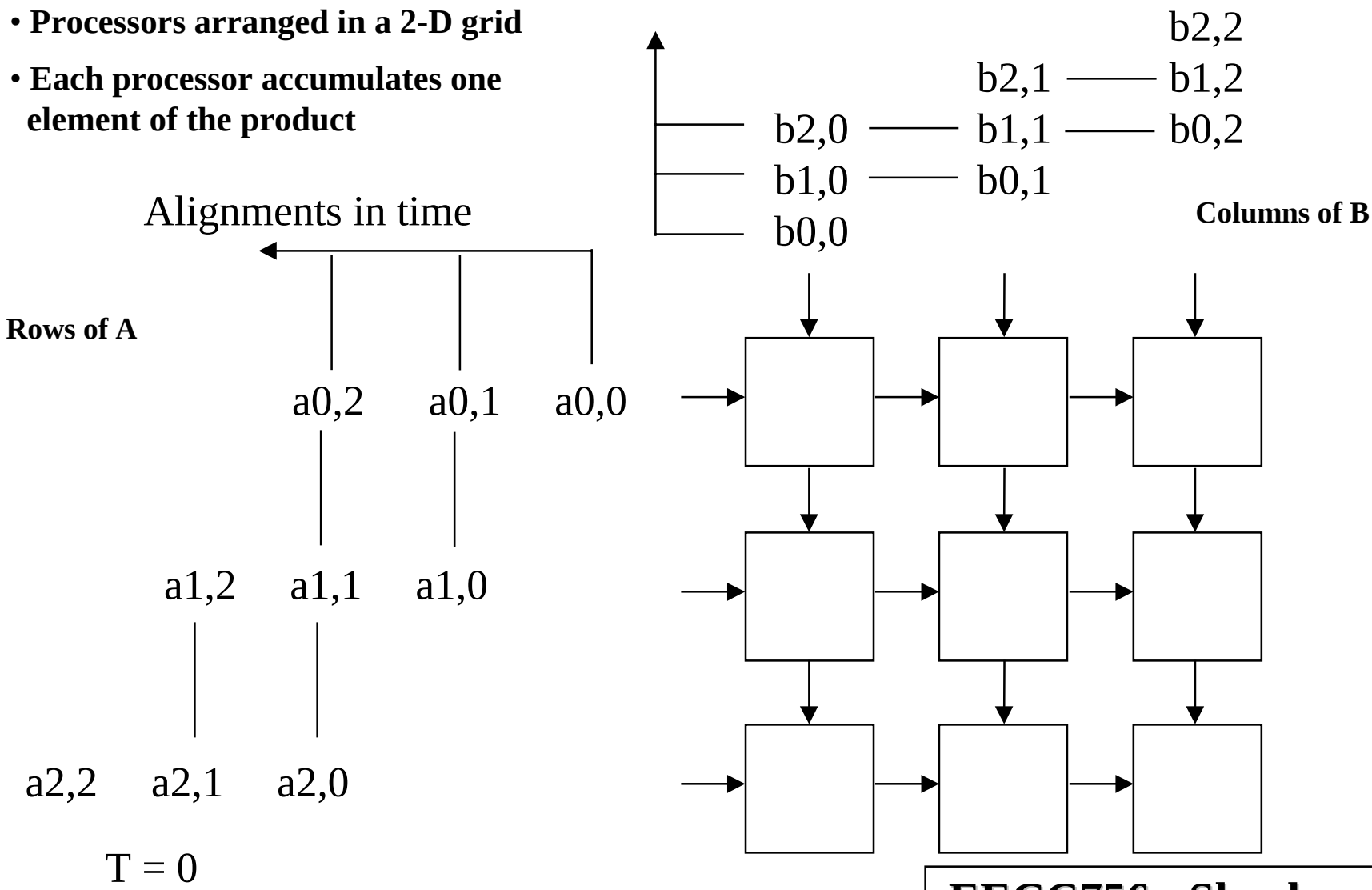
- Replace single processor with an array of regular processing elements
- Orchestrate data flow for high throughput with less memory access




- Different from pipelining
  - Nonlinear array structure, multidirection data flow, each PE may have (small) local instruction and data memory
- Different from SIMD: each PE may do something different
- Initial motivation: VLSI enables inexpensive special-purpose chips
- Represent algorithms directly by chips connected in regular pattern

# Systolic Array Example:
# 3x3 Systolic Array Matrix Multiplication

- **Processors arranged in a 2-D grid**
- **Each processor accumulates one element of the product**




Example source: http://www.cs.hmc.edu/courses/2001/spring/cs156/

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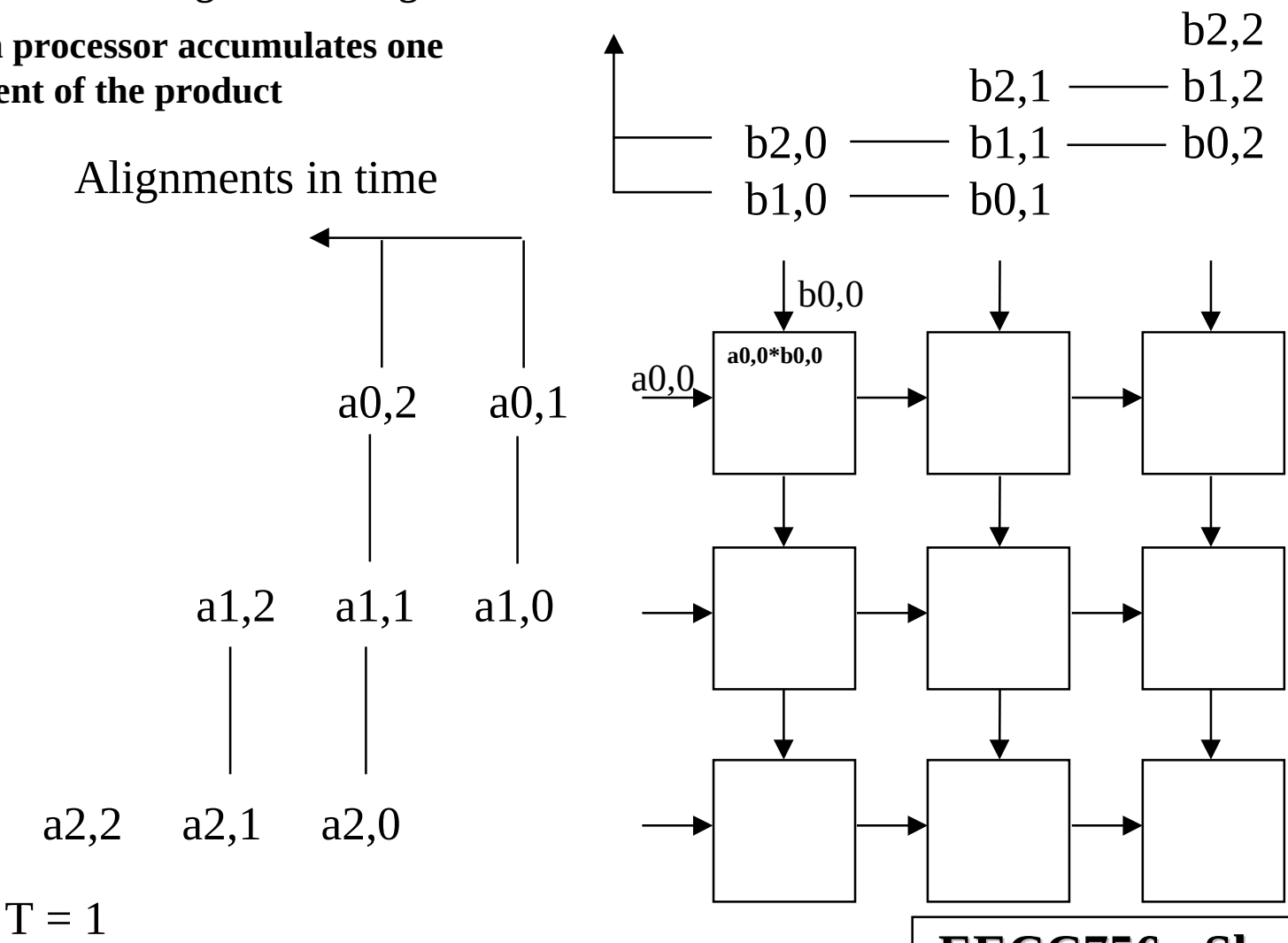

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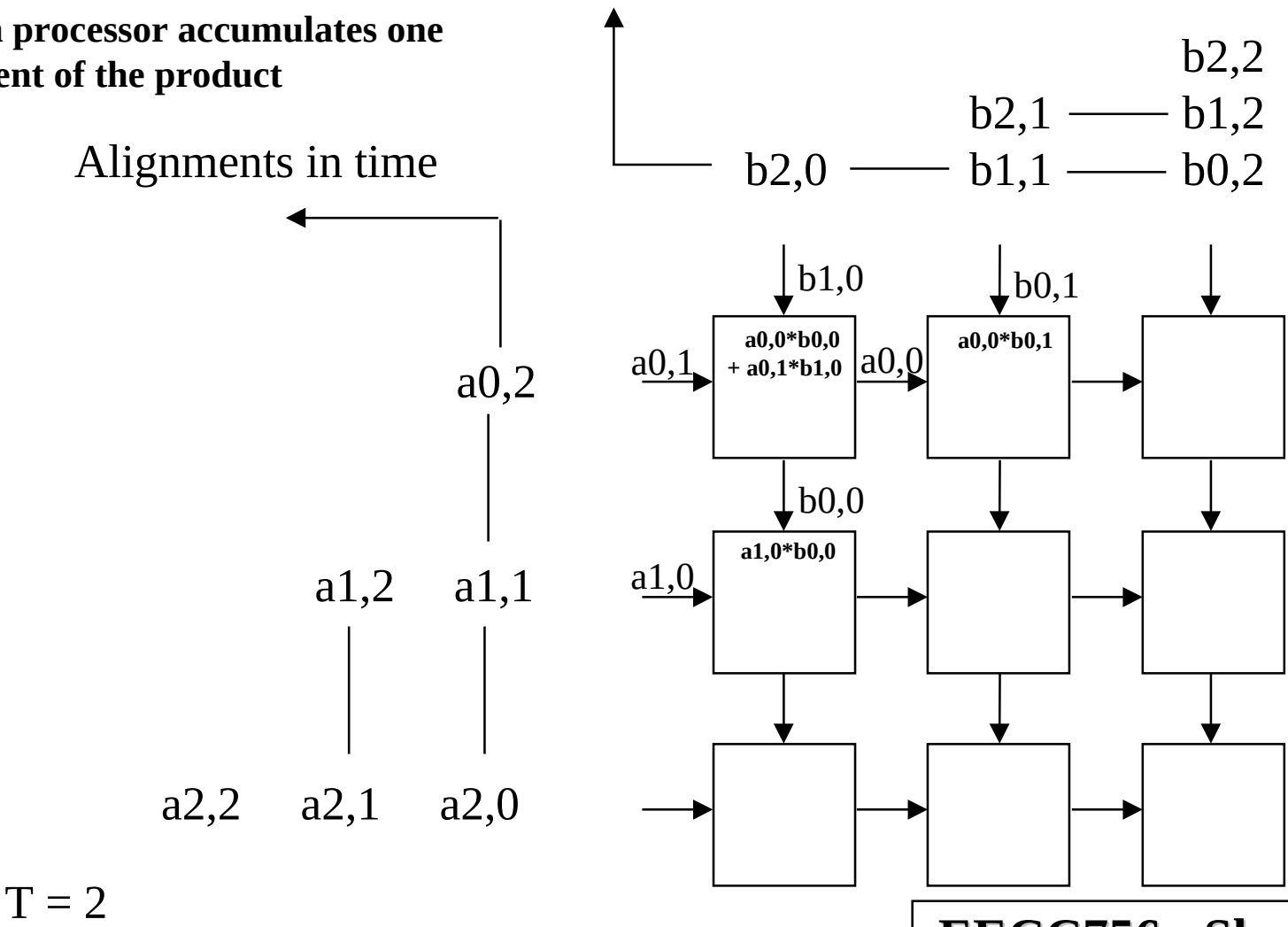


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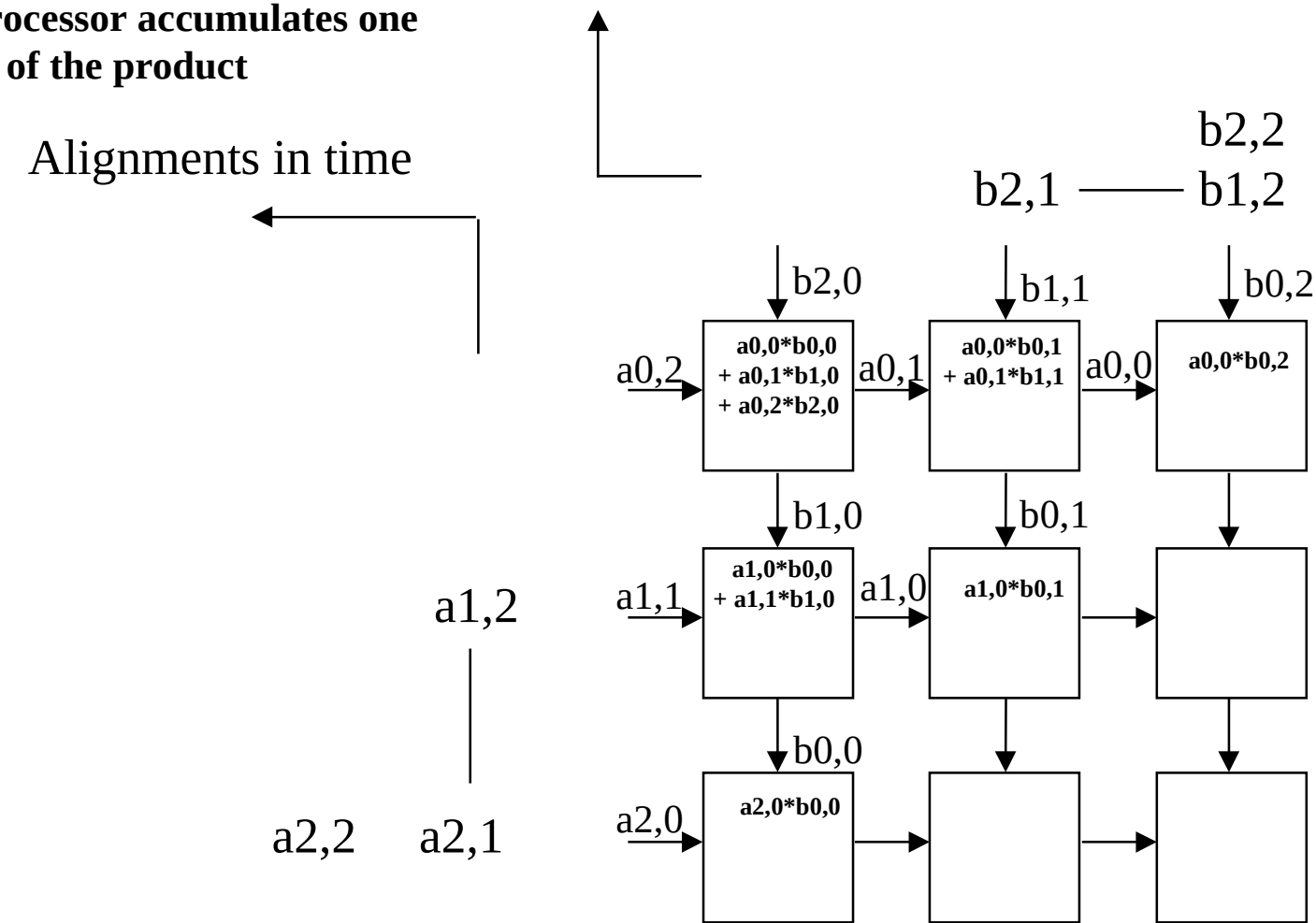


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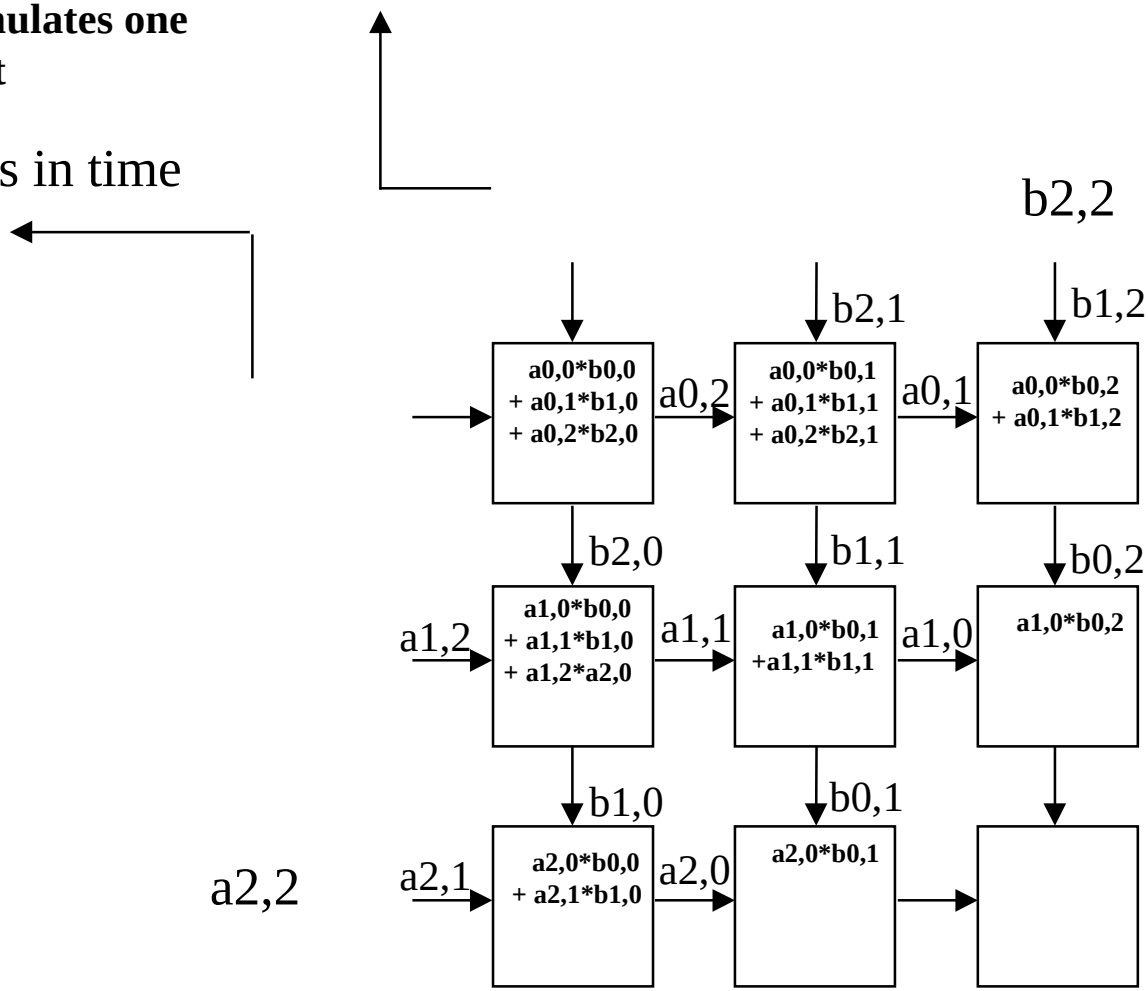


T = 4

**Example source: http://www.cs.hmc.edu/courses/2001/spring/cs156/**

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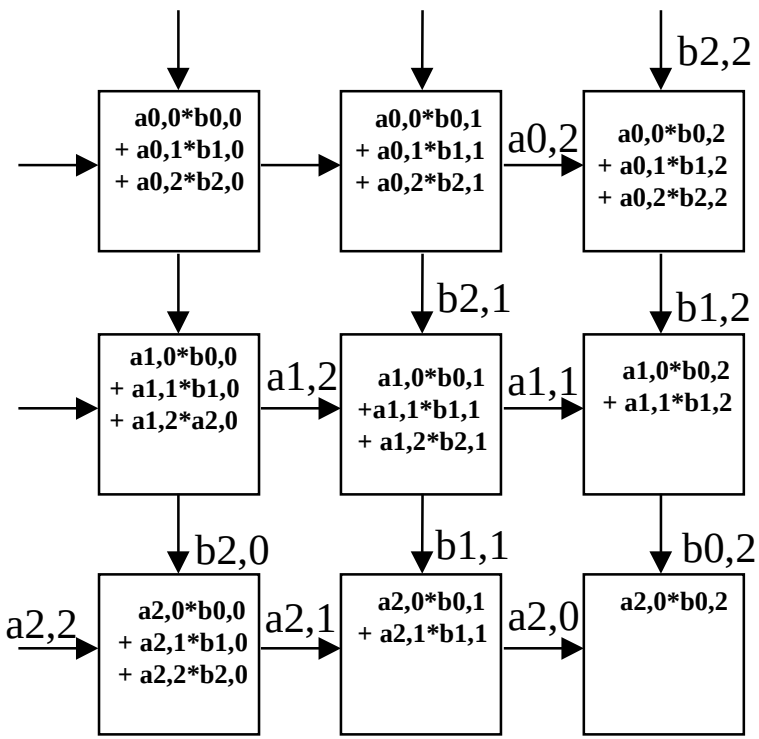
Alignments in time




T = 5

**Example source: http://www.cs.hmc.edu/courses/2001/spring/cs156/**

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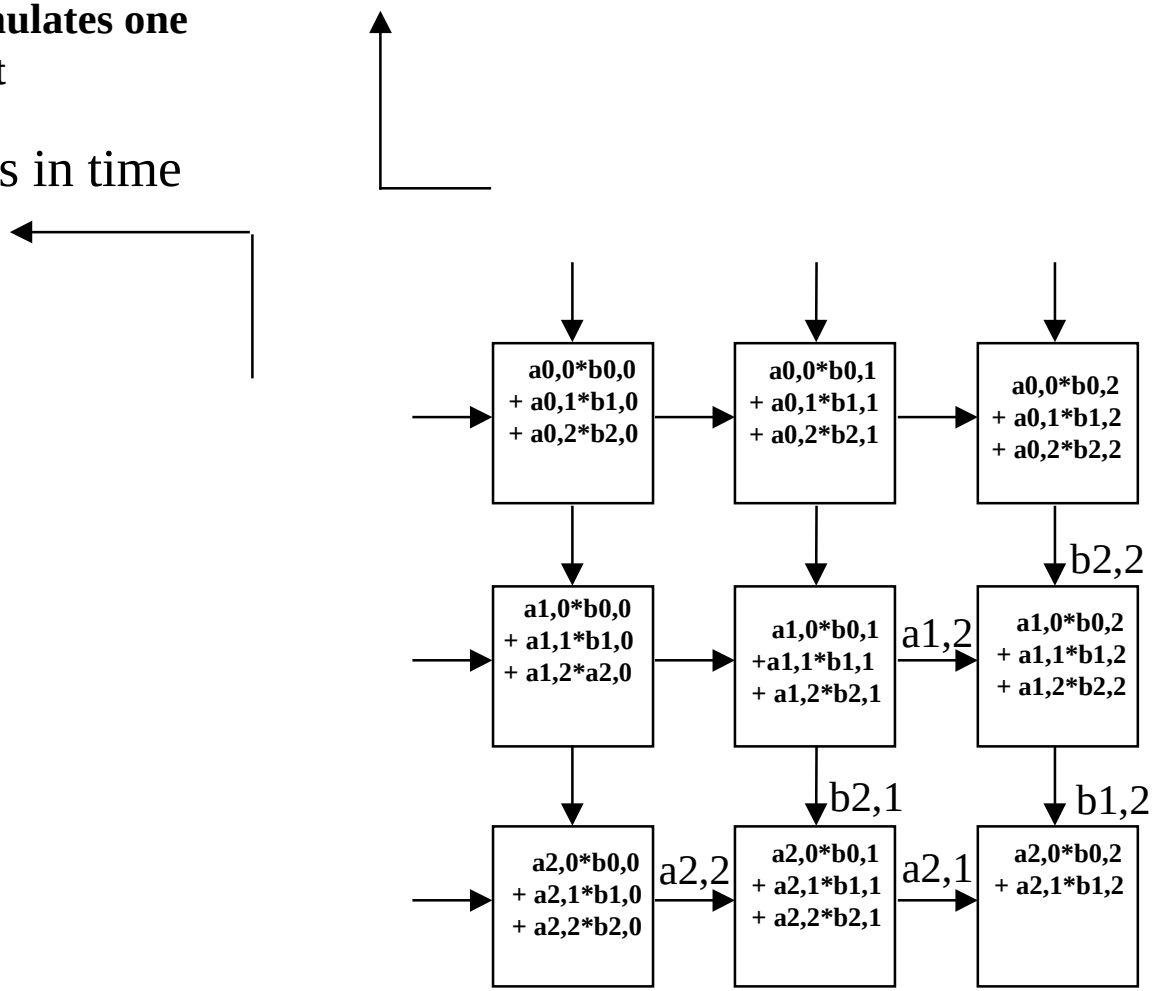


T = 6

**Example source: http://www.cs.hmc.edu/courses/2001/spring/cs156/**

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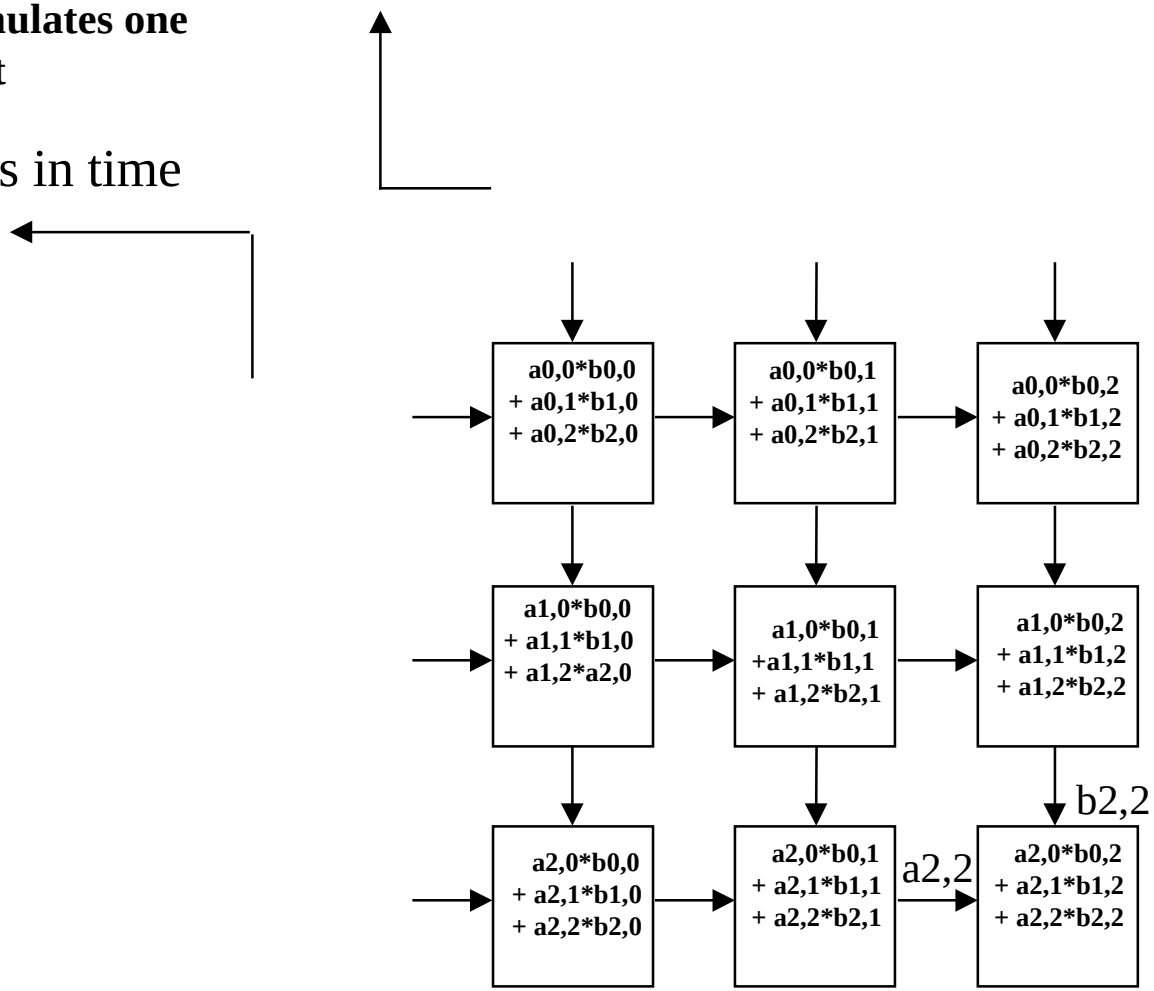


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